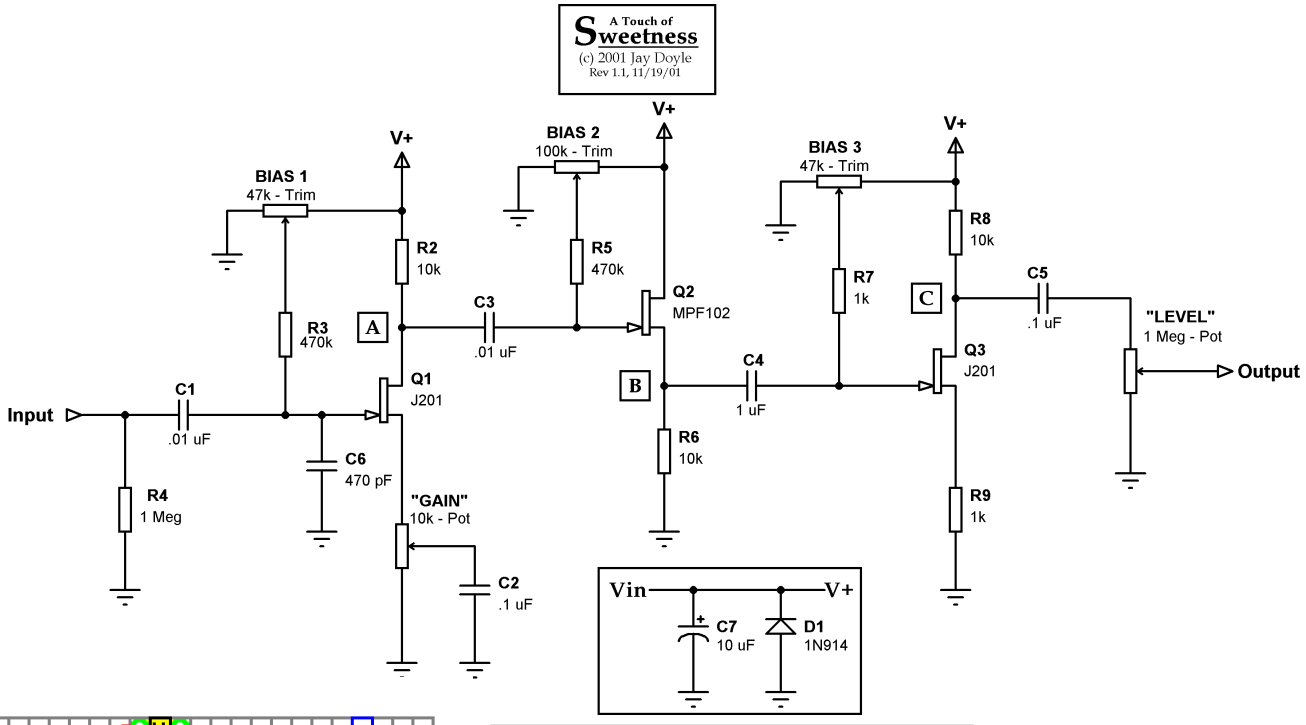
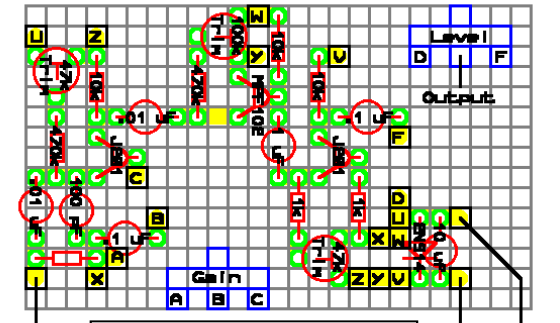
A Touch of Sweetness

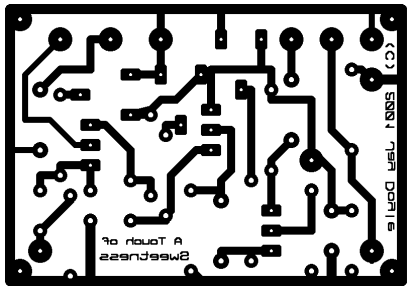
CIRCUIT DESCRIPTION: "A Touch of Sweetness" is an attempt at a mildly distorted, "warm" boost. The circuit takes advantage of the asymmetrical output impedance of a source follower to "squash" the positive swing of the output waveform as well as allowing for higher gain to mild distortion in the upper frequencies. The signal input couples over "bleeder" resistor R4, which removes clicks when using true bypass, through C1 to the gate of Q1. C6 serves to remove RF frequencies and prevent oscillations. Each FET stage employs an input coupling capacitor and a variable gate bias scheme using a trimpot and a 470k-biasing resistor. The resistors are lower than the "Standard" value normally used in an attempt to lower noise and the risk of oscillations. The first transistor, Q1, is set up as a unity gain, inverting amplifier with the ability to raise the gain of upper frequencies, from unity, to the maximum available to the stage by bypassing the source resistor with C2. The headroom of this stage is ½ V+, because the output can only swing from V+, when the FET is "off", to ½ V+, when the FET is all the way "on", due to the divider action of the equal drain and source resistances on Q1. Therefore, the bias voltage at point "A" on the schematic should be set for ¾ V+. Q2 is set up as a simple source follower; point "B" on the schematic should be trimmed to ½ V+. Because the headroom of the stage is nearly the entire voltage supply, the gain is slightly less than unity, and the output voltage of Q1 can not be greater than ½ $V+_{p-p}$, the amount of distortion contributed by Q2 is heavily dependant on the threshold voltage of Q2. Ideally, the threshold voltage would be ½ V+ or greater; the MPF102 FET was chosen because it has a much larger average threshold voltage than the J201. The last stage is a simple common-source amplifier configuration, set up for a gain of about 10. The significant difference is the value of biasing resistor R7. This was chosen (with help from Doug Hammond) to interact with the output impedance of source follower Q2. As a source follower, Q2 pulls hard to V+, allowing for extremely low output impedance, but as the FET "pushes," the only thing pulling it toward ground is the 10k resistor. This makes the output impedance of this half of the signal swing around 10k, getting closer to 10k as it nears ground. R7 interacts with this asymmetry, not effecting the signal on the positive swing, but "rounding off" the negative swing through divider action as the signal swings toward ground. Because Q3 inverts, the "rounded" swing of the signal is the positive swing at the collector of Q3, the bias voltage at point "C" on the schematic should be ≥ ½ V+. I have included layouts for both PCB manufacture or for the smaller perfboard available at Radio Shack.

NOTES: Do not expect a dramatic effect, this circuit offers a "warm" (**NOT** "clean") boost that takes on a crunchy air when using chords or when driven. Three trim-pots and the inter-sample variation among FETs makes this circuit a bit touchy with regards to biasing, it would be best to socket the FETs to try a number of them for the most pleasing sound. As is, the low frequency roll-off of the coupling networks for Q1 and Q2 is about 33 Hz. The coupling network for Q3 rolls off at about 159 Hz. Lowering the value of either the coupling capacitors or the biasing resistors will bring this point higher in the frequency spectrum. The overall gain may be increased by raising the value of R8; Q3's drain resistor. Adjusting the value of R7 will adjust the amount of "rounding" to the output waveform; good values to try are 470Ω to 2k. Raising C2 will allow greater gain across a wider frequency spectrum. The voltages at the bias points determine the amount of clipping, if any, and to some extent adjust the harmonic content of the output signal; for maximum headroom, use the above recommendations. As always, experimentation, after getting it up and running as shown, is encouraged.

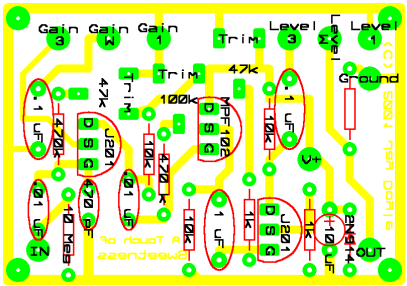




Small RS Perfboard Layout



Layout Shown in 2" x 2.5" Box



Top View